

MSE 4241

Homework #2 (10% of grade)

Due February 17 (NEXT Tuesday) at start of class.

- 1) With regards to an STM tip near a conducting samples surface:
 - a. Plot the current experienced by the atom at the end of an STM tip as it approaches the surface (i.e. as a function of separation).
 - b. On this same plot overlay the current experienced by the next nearest atom (you may assume the apical atom is 1 Angstrom closer to the surface than the '2nd' on the tip).
 - c. If there are 3 such "2nd atoms" (i.e. the tip is a 3-sided pyramid), how much total contribution to the STM signal comes from the apex vs. the combined next neighbors?



NOTE: *You may assume $k=1$. Also state any other assumptions you need to make to answer the question. You may plot the current in arbitrary units if that makes your life easier.*

- 2) Your computer heats up as you use it. In more demanding applications, computer components can heat up substantially (military specs typically require operation in the range from -55C to 125C).
 - a. As a function of temperature over this temperature range, plot the probability of an electron in n-type Si exciting into the conduction band from a Fermi level at 1 eV. It is recommended that you use k_b of 8.617 eV/Kelvin and a bandgap for Si of 1.11 eV.
 - b. What Fermi level is necessary to guarantee that within this temperature range the max probability of electrons exciting into the conduction band will be 1% or less?
- 3) For transistor gates in the years 2001, 2007, and 2016, assuming the gate oxide is SiO₂ with a practical dielectric constant of 3.9:
 - a. Calculate the charge IN ELECTRONS (not Coulombs) on each gate.
 - i. Use the ITRS 2002 roadmap shown in the last few lectures for the rest of the data you will need. Note that the voltage, *physical* gate length, gate width (half pitch or node vals), and effective oxide thickness (lower bound) are all changing.
 - ii. The easiest permittivity value to use is: $\epsilon_0 = 55.3E-6 \text{ e}^-(V*m)$
 - b. Calculate the actual gate thickness if each transistor uses HfO₂ as the gate oxide instead of SiO₂ (dielectric constant of 20 instead of 3.9).
- 4) Discuss 3 technologies for enhancing the spatial resolution (i.e. decreasing the size) of lithographically defined devices (discuss tricks, other methods of lithography, etc).
- 5) Draw band diagrams for a molecule between two metals with no voltage applied, with a positive bias, and with a large positive bias. Sketch the probable I vs V response of this device assuming no sequential tunneling.